WHAT IS CLAIMED IS:

1. A non-volatile memory cell array comprising a first plurality of X-lines configured to be logically identical in a read mode of operation, and each associated with a first Y-line group numbering at least one Y-line.

2. The memory array as recited in claim 1 wherein each of the first plurality of X-lines is also associated with a second Y-line group numbering at least one Y-line.

3. The memory array as recited in claim 2 wherein the first and second Y-Line groups are simultaneously selectable in a read mode and, when so selected, are respectively coupled to true and complement inputs of a sense amplifier circuit.

4. The memory array as recited in claim 3 wherein the first and second Y-line groups each numbers only one Y-line.

5. The memory array as recited in claim 3 wherein the first and second Y-line groups each numbers more than one Y-line.

6. The memory array as recited in claim 3 further comprising a reference signal operably coupled to either the true or complement input of the sense amplifier, wherein the first and second Y-line groups each numbers more than one Y-line.

7. The memory array as recited in claim 6 wherein the reference signal comprises a reference current.

8. The memory array as recited in claim 1 wherein:
the first Y-line group includes more than one Y-line; and
each of the first Y-line group is configured to be logically identical in a read mode of operation.

9. The memory array as recited in claim 1 wherein each of the first plurality of X-lines is logically independent in a write mode of operation.

10. The memory array as recited in claim 1 wherein the memory array comprises passive element memory cells.

11. The memory array as recited in claim 10 wherein the memory array comprises anti-fuse memory cells.

12. The memory array as recited in claim 10 wherein the memory array comprises magnetoresistive memory cells.

13. The memory array as recited in claim 1 wherein the memory array comprises EEPROM memory cells.

14. The memory array as recited in claim 1 wherein the memory array comprises a two-dimensional memory array having one plane of memory cells.

15. The memory array as recited in claim 1 wherein the memory array comprises a three-dimensional memory array having more than one plane of memory cells.

16. The memory array as recited in claim 15 wherein the first plurality of X-lines comprises X-lines disposed on more than one layer of the memory array.

17. The memory array as recited in claim 15 wherein the first plurality of X-lines comprises X-lines disposed on a single layer of the memory array.

18. The memory array as recited in claim 2 configured to perform threshold logic upon one or more inputs to the array.

19. The memory array as recited in claim 1 further comprising a second plurality of X-lines configured to be logically identical in a read mode of operation and each associated with the first Y-line group.

20. The memory array as recited in claim 19 further comprising a third plurality of X-lines associated with the first Y-line group, said third plurality of X-

lines being configured, in a read mode of operation, to be logically identical with each other and complementary to the first plurality of X-lines.

21. The memory array as recited in claim 20 further comprising:

a fourth plurality of X-lines associated with the first Y-line group, said fourth plurality of X-lines being configured, in a read mode of operation, to be logically identical with each other and complementary to the second plurality of X-lines; and

a second Y-line group numbering at least one Y-line, each of which is associated with the first, second, third, and fourth pluralities of X-lines.

22. The memory array as recited in claim 19 configured to perform threshold logic upon one or more inputs to the array.

23. The memory array as recited in claim 19 configured to perform weighted input threshold logic upon one or more inputs to the array.

24. The memory array as recited in claim 1 wherein X-lines comprise word lines.

25. The memory array as recited in claim 1 wherein X-lines comprise bit lines.

26. The memory array as recited in claim 1 configured as a content addressable memory array.

27. The memory array as recited in claim 2 wherein:

each of the first Y-line group is configured to be logically identical in a read mode of operation; and

each of the second Y-line group is configured to be logically identical in a read mode of operation.

28. The memory array as recited in claim 1 embodied in computer readable descriptive form suitable for use in design, test or fabrication of an integrated circuit.

29. A method of operating a non-volatile memory array comprising:

programming individual memory cells associated with a first X-line group of at least one X-line and further associated with a first Y-line group of at least one Y-line until a desired first aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the first group of Y-lines; and

reading the memory array by simultaneously selecting all the first group of X-lines and all the first group of Y-lines and generating a signal responsive to the first aggregate memory cell read current.

30. The method of claim 29 further comprising:

programming individual memory cells associated with the first X-line group and further associated with a second Y-line group of at least one Y-line until a desired second aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the second group of Y-lines, which second aggregate memory cell current is greater than the first aggregate memory cell current; and

reading the memory array by simultaneously selecting all the first group of X-lines and all the first and second groups of Y-lines and generating a signal responsive to the greater of the first and second aggregate memory cell read current.

31. The method of claim 30 wherein the memory array comprises write-once memory cells.

32. The method of claim 29 further comprising:

programming more than one cell associated with an X-line by simultaneously activating at least two Y-lines.

33. The method of claim 32 wherein said at least two simultaneously activated Y-lines are associated with different Y-line groups.

34. The method of claim 29 wherein the memory array comprises passive element memory cells.

35. The method of claim 34 wherein the memory array comprises anti-fuse memory cells.

36. The method of claim 34 wherein the memory array comprises magnetoresistive memory cells.

37. The method of claim 29 wherein the memory array comprises EEPROM memory cells.

38. An integrated circuit comprising:

a memory array including:

a plurality of X-lines disposed on at least one layer of the memory array;

a plurality of Y-lines disposed on at least one other layer of the memory array;

a plurality of non-volatile memory cells, each coupled to an associated one of the plurality of X-lines and an associated one of the plurality of Y-lines;

an X-line selection circuit for selecting at least a first X-line group of at least two X-lines when in a read mode, and for selecting a lesser number of X-lines within at least the first X-line group when in a write mode; and

a Y-line selection circuit for simultaneously selecting in the read mode a first Y-line group of at least one Y-line and a second Y-line group of at least one Y-line, and for respectively coupling the selected first and second Y-line groups to respective first and second inputs of an associated sense amplifier circuit;

wherein the associated sense amplifier circuit is responsive to an aggregate signal from memory cells associated with both the selected first X-line group and the selected first Y-line group, and responsive to an aggregate signal from memory cells associated with both the selected first X-line group and the selected second Y-line group.

39. The integrated circuit as recited in claim 38 further comprising a reference signal circuit operably coupled to the second input of the associated sense amplifier circuit.

40. The integrated circuit as recited in claim 38 wherein the first Y-line group and the second Y-line group each number but one Y-line.

41. The integrated circuit as recited in claim 38 wherein the associated sense amplifier circuit is configured to sense more than two levels of aggregate memory cell signal.

42. The integrated circuit as recited in claim 38 wherein:

the X-line selection circuit is further configured for selecting, when in the read mode, a second X-line group of at least two X-lines simultaneously with selecting the first X-line group; and,

the associated sense amplifier circuit is responsive to an aggregate signal from memory cells associated with the selected first X-line group and the selected first Y-line group and memory cells associated with the selected second X-line group and the selected first Y-line group, and responsive further to an aggregate signal from memory cells associated with the selected first X-line group and the selected second Y-line group and memory cells associated with the selected second X-line group and the selected second Y-line group.

43. The integrated circuit as recited in claim 38 wherein:

the X-line selection circuit is further configured for selecting, when in the read mode, a third X-line group of at least two X-lines whenever the first X-line group is not selected.

44. The integrated circuit as recited in claim 38 wherein the memory array comprises passive element memory cells.

45. The integrated circuit as recited in claim 44 wherein the memory array comprises anti-fuse memory cells.

46. The integrated circuit as recited in claim 38 wherein the memory array comprises EEPROM memory cells.

47. The integrated circuit as recited in claim 38 wherein the memory array comprises a three-dimensional memory array having more than one plane of memory cells disposed above a semiconductor substrate.

48. The integrated circuit as recited in claim 47 wherein the first X-line group comprises X-lines disposed on more than layer of the memory array.

49. The integrated circuit as recited in claim 47 wherein the first X-line group comprises X-lines disposed on a single layer of the memory array.

50. The integrated circuit as recited in claim 38 embodied in computer readable descriptive form suitable for use in design, test or fabrication of said integrated circuit.

51. An integrated circuit comprising:

a memory array including:

a plurality of X-lines disposed on at least one layer of the memory array;

a plurality of Y-lines disposed on at least one other layer of the memory array;

a plurality of non-volatile memory cells, each coupled to an associated one of the plurality of X-lines and an associated one of the plurality of Y-lines;

means for programming individual memory cells associated with a first X-line group of at least one X-line and further associated with a first Y-line group of at least one Y-line until a desired aggregate memory cell read current is obtained when simultaneously selecting all the first group of X-lines and all the first group of Y-lines; and

means for reading the memory array by simultaneously selecting all the first group of X-lines and all the first group of Y-lines and generating a

signal responsive to the aggregate memory cell read signal conveyed on the first group of Y-lines.

52. The integrated circuit of claim 51 further comprising:

means for programming more than one cell associated with an X-line by simultaneously activating at least two Y-lines.

53. The integrated circuit of claim 52 wherein said at least two simultaneously activated Y-lines are associated with different Y-line groups.

54. The integrated circuit of claim 51 wherein the memory array comprises passive element memory cells.

55. The integrated circuit of claim 54 wherein the memory array comprises anti-fuse memory cells.

56. The integrated circuit of claim 51 wherein the memory array comprises EEPROM memory cells.